An optimized quantum circuit for converting from sign-magnitude to two's complement

F. Orts · G. Ortega · E.M. Garzón

Abstract Nowadays, one of the critical issues to implement quantum algorithms is the required number of elementary gates, qubits and delay. Current quantum computers and simulators are mainly prototypes and there is a lack of computational resources. Therefore, it is necessary to optimize the quantum operations to reduce the necessary number of gates and qubits. This work presents a novel reversible circuit which is able to convert signed binary numbers to two's complement of N digits in a quantum environment. The depth of the circuit is O(log N). It is based on the fastest out-of-place carry look-ahead addition quantum circuit currently available. This addition circuit has been adapted to make the conversion using the minimum number of gates and qubits, being faster than other adder circuits. A robust metric has been used to measure the quantum cost, delay, ancilla inputs and garbage outputs of the proposed converter. Moreover, it has been compared with others described in the literature.

1 Introduction

Quantum computers are based on reversible gates as they must satisfy the principles of quantum mechanics, for example, the reversibility [26]. There is a

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wide variety of literature about building circuits in quantum computers using reversible gates, especially circuits related to arithmetic operations. For instance, there is a special interest in getting faster arithmetic reversible gates to be used as a module in Shor's algorithm. There are optimized gates to compute addition [6,36], subtraction [25,28,35], multiplication [4,8] and division [11,27].

However, the optimization of arithmetic gates is not the only way to improve these circuits. Sometimes, it can be done with new high-level approaches, like using different formats to represent the information. For example, the two's complement is the way how classic computers represent integers to simplify the hardware for additions and subtractions [1]. In terms of quantum computers, adder circuits are faster than subtractor ones [35,36]. Focusing our attention on the two's complement, subtractions can be computed as additions.

In this work, a circuit to convert from signed binary numbers to two's complement is presented. The design of a two's complement quantum converter can be based on quantum gates or quantum adders that compute $\bar{a} + 1$. Our proposal is based on the most optimized state-of-the-art adder circuits for quantum computers since they improve the converter circuits based on quantum gates in terms of delay. The conversion from a signed binary number, a, to two's complement can be computed as $\bar{a} + 1$ [13]. It can be done negating each digit of a and using an adder to compute $\bar{a} + 1$. The best quantum adders in terms of cost and depth are proposed in [6,36]. They are considered as the start point to design a specific adder to compute $\bar{a} + 1$.

The rest of the work is presented as follows: Section 2 details popular metrics to evaluate a quantum circuit. Section 3 describes the state-of-the-art converter circuits. Section 4 presents the proposed circuit, and Section 5 compares the proposed circuit with respect to the state-of-the-art converter circuits described in Section 3. Finally, Section 6 summarizes the conclusions.

2 Measures in a quantum circuit

The metric described in [22] has been adopted in this work. This metric defines four important factors to measure a circuit in terms of efficiency:

- Number of ancilla inputs: constant inputs used to perform auxiliary operations.
- Garbage outputs: outputs which cannot be used at the end of the circuit since it is impossible to know their values. Unless these garbage outputs were reversibly removed (uncomputed), such outputs (qubits) may not be be used later, which would result in a waste of resources. So, if they were entangled with inputs of other circuits, they would produce uncertain results [26].
- Delay: the logical depth of the circuit. It is an important parameter which is related to the efficiency of the circuit [35]. In [22], $\triangle$ is defined as the delay unit.
- Quantum cost: number of gates.

It is necessary to underline that not all gates have a similar size. For instance, it is unfair to consider the Pauli-X gate [41] and the Toffoli gate [38] are similar in terms of quantum cost or delay, as the Toffoli gate involves 5 2×2 gates (2 Controlled-V gates, 1 Controlled-V^+ gate [9] and 2 controlled-NOT (CNOT) gates) [26] and Pauli-X gate is one 1×1 gate. So, [22] sets the delay according to the size of the gates. This metric has also been considered in this work. Authors in [22] set the delay of 1×1 and 2×2 gates to 1△, and the delay of an $N×N$ gate is calculated as its depth when it is built using 1×1 and 2×2 gates. Moreover, the quantum cost of a circuit depends on its number of gates with delay 1△. For instance, as Toffoli gate has 5 2×2 gates, it has a quantum cost of 5 and a delay of 5△ (as no operations can be done simultaneously).

It is relevant to underline that different physical realizations have been explored to develop quantum circuits. At those levels of abstraction, the evaluation metrics can also focus on other parameters. For instance, in linear optics, there is a special interest in optimizing the number of controlled-unitary gates since the CNOT gate can only be probabilistically implemented. There are several works focused on optimizing the number of needed CNOT gates to implement the Toffoli gate as it is one of the most used. In [14], authors introduced a new implementation of the Toffoli gate using only two CNOT gates and one generalized controlled-PHASE gate. Another version of the Toffoli gate was presented in [15], with an optimized controlled-PHASE gate. This last version has only three two-qubits gates. It is the best option in terms of the number of two-qubits gates.

For the sake of clarity, the symbols of the used gates are shown in Figs. 1, 2, 3 and 4. According to [22], the Pauli-X and the CNOT gates have a quantum cost of 1 and a delay of 1△. As it was mentioned in the previous paragraph, according to [22] the Toffoli gate has a quantum cost of 5 (three two-qubits gates according to [15]) and a delay of 5△. The Peres gate is built with two Controlled-V^+ gates, a Controlled-V gate, and a CNOT gate. Therefore, it has a quantum cost of 4 and a delay of 4△.
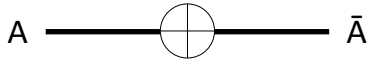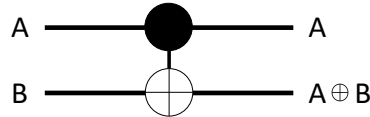

Fig. 1 Symbol of the Pauli-X gate.
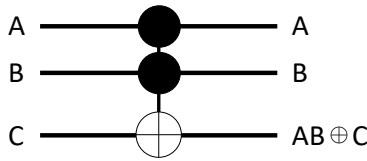

Fig. 2 Symbol of the CNOT gate.

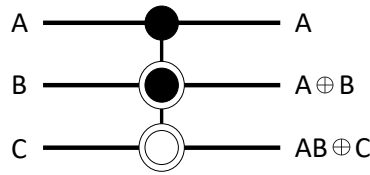**Fig. 3** Symbol of the Toffoli gate.

Fig. 4 Symbol of the Peres gate.

3 Methodology to design two's complement converters

The two's complement of an N-digit number is its complement with respect to 2^N. The range of numbers in a two's complement system is $-(2^{N-1}) \leq a \leq (2^{N-1} - 1)$ [13]. For instance, Table 1 shows the conversion of a number a from signed binary to two's complement when $N = 4$. Converting a number a from signed binary to two's complement is as follows. If $a >= 0$, no conversion is necessary because both representations, signed binary and two's complement, of a are equal. However, if $a < 0$, the conversion is necessary. It can be calculated as the inversion of all the digits of a and then to compute $\bar{a} + 1$.

There are two approaches to convert signed binary numbers to two's complement of N digits in a quantum environment. One of them consists of designing a specific circuit for such purpose and the another one is considering available addition circuits for the conversion.

Signed binary number	Two's complement
0111	7
0110	6
0101	5
0100	4
0011	3
0010	2
0001	1
0000	0
1111	-1
1110	-2
1101	-3
1100	-4
1011	-5
1010	-6
1001	-7
1000	-8

Table 1 Signed and Two's complement representation of binary numbers with $N = 4$.

There are several proposals in the literature which follow the approach based on designing a specific circuit. In [30], authors mathematically propose a new gate, called $SSMT$ gate, to compute the conversion of a 4-digit number. In [2], a quantum gate called TCG is proposed. In a similar way than the previous $SSMT$ gate, it performs the conversion of a 4-digit number ($N = 4$). The TCG gate is also used (and optimized) in [3], and it achieves the best quantum cost (25) for the case $N = 4$. However, it is not possible to join several TCG gates to compute the two's complement of any number with more than 4 digits. The reason is that the TCG gate does not handle either input or output carries. Besides, it only computes the truth table for the 4-digit case.

Other approaches in the literature are based on using existing addition circuits. This strategy is more widely used because this kind of circuits are

more efficient in terms of delay than the specific converter circuits. As it has been mentioned, the conversion can be computed as the inversion of all the digits of a and then $\bar{a}+1$, so it is only necessary to invert each digit of a with N Pauli-X gates and then to use an existing addition circuit to compute $\bar{a}+1$. There are several papers about quantum addition circuits of two integers [5, 6, 19, 31–33], which is one of the most important basic operations. The two most efficient addition circuits are [6, 36], with a delay of O($\log N$).

The circuit proposed in this work is based on the circuit presented in [36]. However, instead of using this circuit in a direct way to compute $\bar{a}+1$, it has been adapted and improved to compute the conversion from signed numbers to two's complement. The details of the proposed circuit are presented in the next section.

4 Proposed Two's Complement Converter

As it has been mentioned in the previous section, the proposal circuit is an adaptation of a reversible out-of-place carry look-ahead adder presented in [36]. The objective is to perform $\bar{a}+1$ (assuming that a is a negative number in signed binary format). The mentioned adder performs the operation between two numbers, so if we consider a and $b=1$, it is only necessary to apply a Pauli-X gate to each digit of a at the beginning and the conversion could be done. However, taking into account that b is always 1, several improvements can be done in order to reduce the original circuit.

The converter improves the delay performing g_i and p_i in parallel when possible (being $g_i = a_i b_i$ and $p_i = a_i + b_i$, according to the notation given by [17]) and removing or simplifying the operations related to b, since $b=1$. It uses N ancilla qubits (Zg_i) to allocate the sum S_{i+1}. It also needs extra ancilla qubits (Zp_i) to store propagated carry values, which are restored to 0 at the end of the circuit to avoid garbage outputs. Since $b=1$, the qubits used to represent b in [36] are deleted except the least significant one.

The first change to apply with respect to [36] is to include several Pauli-X gates to transform a into $\bar{a}$. The second change consists of removing the first Toffoli gate (quantum cost 5 according to [26], three two-qubits gates according to [15]) and replacing it with a CNOT gate (quantum cost 1). This can be done as the Toffoli gate computes $a_0 b_0 \oplus Zg_0$, which is always $a_0 \oplus Zg_0$ if $b_0 = 1$. Thirdly, the $(N-1)$ Peres gates (quantum cost 5) can be removed from the circuit. The i-Peres gate computes $a_i \oplus b_i$ in its second qubit, which is always a_i if $b_i = 0$. Also, the i-Peres gate computes $a_i b_i \oplus Zg_i$ in its third qubit, which is always Zg_i if $b_i = 0$. The Peres gates have a quantum cost of 5, so this step reduces the quantum cost in 5 for each removed gate, that is, $5(N-1)$. Moreover, [36] applies Toffoli gates at locations Zg_i, b_i and Zg_{i+1} for $i = 2$ to $N/2$. All these Toffoli gates except the first one can be removed since, for the case $b = 1$, $Zg_i = 0$ when $i > 2$. This reduces the quantum cost in $(N/2 - 1) \times 5$ and the delay in $5\triangle$ (the remaining gates can be computed in parallel).

As above mentioned, the inputs of b can be removed except the first one, since the other values are always 0. The b_0 digit can be converted into an ancilla input of value 0 inverted with a Pauli gate at the same time that the digits of a. By this way, the number of qubits is reduced by $N - 1$. All the CNOT gates applied at the end to restore the qubits of b can be deleted (except the one which acts over the new ancilla qubit), so a reduction of $N - 1$ CNOT gates is applied. However, as the a_i-inputs have been inverted, a new inversion is required at the end of the circuit to evade garbage outputs. This adds $1\triangle$ to the global delay, but this operation would be also necessary for the original circuit if it worked with two's complement. The remaining gates on which b_i acts as a control qubit are modified so that the new control qubit was a_i.

This way, the idea is to design a reversible look-ahead adder to compute the particular addition $\bar{a} + 1$. The recurrence relation of a general look-ahead adder to accelerate the computation of the carries is well-known [17]. It can be simplified for our particular adder and the addition can be computed as follows:

$$
\begin{aligned}
S_0 &= \overline{a_0} \oplus 1 \\
S_1 &= \overline{a_1} \oplus \overline{a_0} \\
&\cdots \\
S_n &= \overline{a_N} \oplus \overline{a_0}\ \overline{a_1} \ldots \overline{a_{N-1}}
\end{aligned}
\tag{1}
$$

where the term $C_i = \overline{a_0}\ \overline{a_1} \ldots \overline{a_{i-1}}$ represents the carry to compute $S_i = \overline{a_i} \oplus C_i$.

The proposed circuit to compute $\bar{a} + 1$ for an example of $N = 8$ is shown in Fig. 5. The design of such circuit can be explained with the following eight steps.

- **Step 1:** The first step is to transform a into $\bar{a}$ and also to specify b. The input b is supplied by an auxiliary qubit ($b_0 = 1$), instead of the N qubits of [36]. These operations can be done using Pauli-X gates and deleting the $N - 1$ qubits of b. It consists of 9 Pauli-X gates (quantum cost $1 \times 9 = 9$), and it has a delay of $1\triangle$.
- **Step 2:** It is the start point since its output is $\alpha_0 = \overline{a_0}$ which is involved in the generation of all the carry-look ahead formation process. It consists of 1 CNOT gate (quantum cost 1), and it has a delay of $1\triangle$.
- **Step 3:** The outputs of this step are $\alpha_1 = \overline{a_0}\ \overline{a_1}$, $\alpha_2 = \overline{a_2}\ \overline{a_3}$, $\alpha_3 = \overline{a_4}\ \overline{a_5}$ and $\alpha_4 = \overline{a_6}\ \overline{a_7}$. This way, the carry C_1 is computed and also the intermediate AND operations to compute the following carries. This stage consists of 4 Toffoli gates (quantum cost $5 \times 4 = 20$ according to [26], two-qubits gates $3 \times 4 = 12$ gates according to [15]) and it has a delay of $5\triangle$ (all the gates of this step can be computed in parallel).
- **Step 4:** This stage only computes two outputs, $\beta_1 = \overline{a_0}\ \overline{a_1}\ \overline{a_2}\ \overline{a_3}$ and $\beta_2 = \overline{a_4}\ \overline{a_5}\ \overline{a_6}\ \overline{a_7}$. Therefore, $C_4 = \beta_1$ is ready to compute S_4. It consists of 2 Toffoli gates (quantum cost $5 \times 2 = 10$ according to [26], two-qubits gates $3 \times 2 = 6$ according to [15]) with a delay of $5\triangle$ (the 2 gates can be computed in parallel).

- **Step 5:** This step computes $\delta_1 = \overline{a_0}\,\overline{a_1}\ldots\overline{a_7}$ and $\delta_2 = \overline{a_0}\,\overline{a_1}\ldots\overline{a_5}$. Thus, C_6 and C_{out} are computed. This step involves 2 Toffoli gates (quantum cost $5 \times 2 = 10$ according to [26], two-qubits gates $3 \times 2 = 6$ according to [15]) and it has a delay of $10\triangle$.
- **Step 6:** In this step, $\theta1 = \overline{a_0}\,\overline{a_1}\,\overline{a_2}$, $\theta2 = \overline{a_0}\,\overline{a_1}\ldots\overline{a_4}$ and $\theta3 = \overline{a_0}\,\overline{a_1}\ldots\overline{a_6}$ are computed. Hence, $C_3 = \theta1$, $C_5 = \theta2$ and $C_7 = \theta3$ are ready to compute the corresponding sums. Moreover, $R_0 = 0$ is the result of uncomputing β_2, avoiding a garbage output. This step consists of 4 Toffoli gates (quantum cost $5 \times 4 = 20$ according to [26], two-qubits gates $3 \times 4 = 12$ according to [15]) and a delay of $5\triangle$ (all the gates of this step can be computed in parallel).
- **Step 7:** $R_1 = 0$, $R_2 = 0$ and $R_3 = 0$ are the result of uncomputing α_2, α_3 and α_4, respectively. Consequently, all the auxiliary inputs have been uncomputed. It consists of 3 Toffoli gates (quantum cost $5 \times 3 = 15$ according to [26], two-qubits gates $3 \times 3 = 9$ according to [15]) and a delay of $5\triangle$ (the 3 Toffoli gates can be computed in parallel).
- **Step 8:** In this stage the sums can be calculated since the carries C_i have been computed. So, the output sum is complete at this step. This step consists of 8 CNOT gates (quantum cost $1 \times 8 = 8$) and a delay of $1\triangle$ (all the CNOT gates can be computed in parallel).
- **Step 9:** The qubits of a are restored to their input values to avoid garbage outputs. It consists of 8 Pauli-X gates (quantum cost $1 \times 8 = 8$) and a delay of $1\triangle$ (all the Pauli-X gates can be computed in parallel).

Therefore, the quantum cost of the converter for $N = 8$ is 101 (54 controlled-unitary gates if the Toffoli gate of [15] is used) and the delay is $34\triangle$. An analogous design can be carried out for a generic N value with a quantum cost of $21N - 15w(N) - 15log(N - 4)$ ($w(N)$ represents the number of ones in the binary expansion of N) and a delay of $logN + logN/3 + 1$.

5 Results and discussion

In this section, the state-of-the-art circuits are analyzed in order to justify the selection of [36] as the start point to design the converter. This analysis is based on the widely used methodology introduced in [22]. Finally, the obtained results by the proposed converter are compared with the results of the most efficient state-of-the-art circuits.

5.1 Revision of modern quantum adders

After papers [6,36] were published, other adders have been proposed but none of them has improved them in terms of delay and cost. A reversible 16 digit carry-look-ahead adder is proposed in [40]. It consists of 72 CNOT gates and 96 Toffoli gates with a total quantum cost of 552. Several works propose new designs of ripple-carry adder circuits [20,23,39], but the delay of this kind
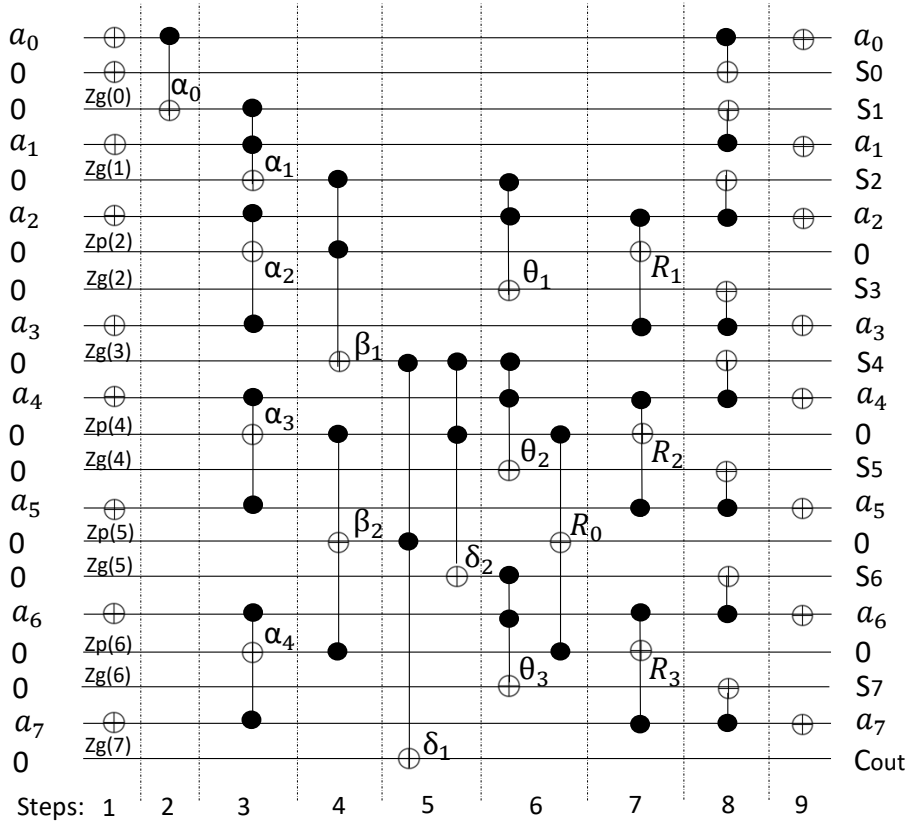
Fig. 5 Design of the converter for a 8-digit number. a_i are the qubits of the input number, $Zg(i)$ will contain S_{i+1} (the result) at the end, and $Zp(i)$ are auxiliary qubits used to store propagated carry value for intermediate digits (they are uncomputed at the end).

of adders is longer than the carry-look-ahead adder circuits [10]. A quantum adder based on genetic algorithms is proposed in [16], which is not comparable since it uses an alternative methodology. The proposal introduced in [34] does not achieve improvements in the terms studied in Section 2, but it gives valuable information about fault tolerant techniques in adder circuits. On the other hand, there are several works in which additions and subtractions are computed using the same circuit [7,12,21,24,37]. Although they are able to compute both operations, they are less competitive than [6,36] in terms of delay and quantum cost, due to the extra cost of performing both operations, as it is shown in Table 7 of [24].

In [29], a new adder circuit which optimizes the number of gates and depth is presented (see Fig. 6). It is built using Peres and CNOT gates, with a quantum cost of $2 \times N \times 4 + (N \times 1)$, which is better than the circuit we present even including the extra cost of $2 \times N$ necessary to the inversion and restoration of the a inputs. However, in the proposal of [29], the garbage outputs have not
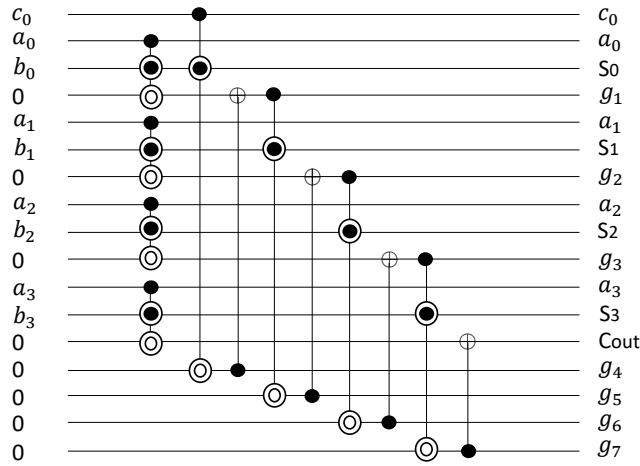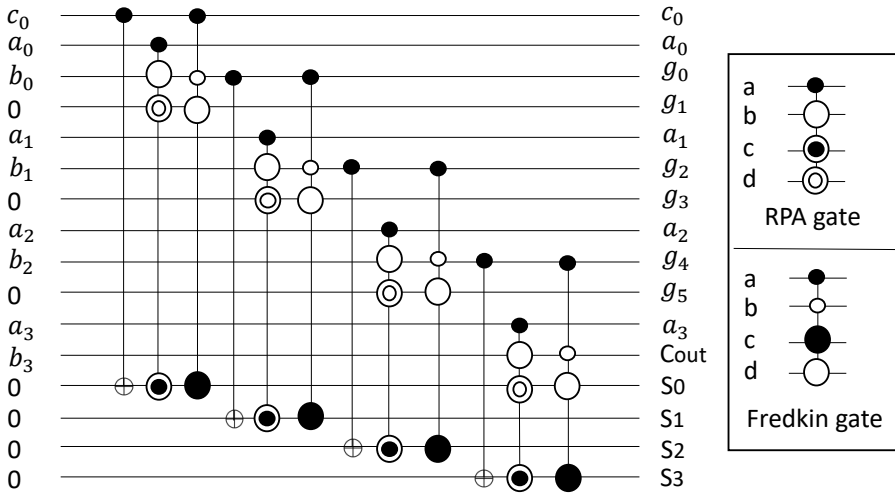
Fig. 6 First carry-look-ahead quantum adder design proposed in [29]. a_i and b_i are the input numbers, c_0 is the carry input, S_i are the qubits of the result, C_{out} is the carry output and g_i are garbage outputs with an unknown output.
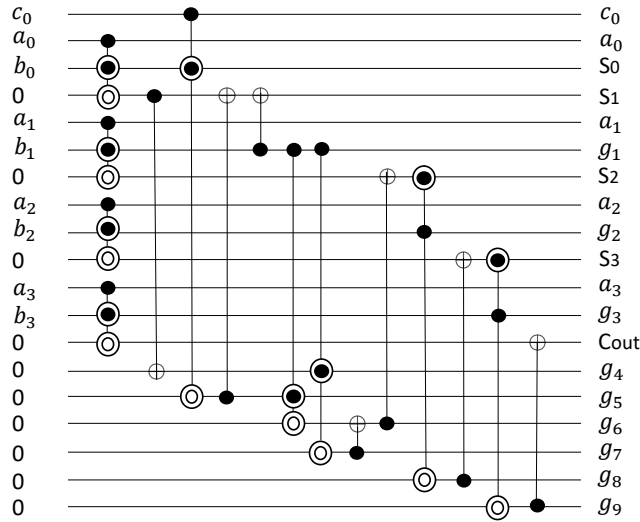
Fig. 7 Second carry-look-ahead quantum adder design proposed in [29]. a_i and b_i are the input numbers, c_0 is the carry input, S_i are the qubits of the result, C_{out} is the carry output and g_i the garbage outputs with an unknown output.

been uncomputed (g outputs in Fig.6). As it was mentioned in Section 2, these garbage outputs cannot be used later and it is a waste of resources. The circuit has $3 \times N$ garbage outputs. Notice that uncomputation will increase the number of gates and the depth of the circuit [26], so the numbers given in Table 3 of [29] need to be revised. On the other hand, they consider any output which is not part of the result is garbage output, uncomputed or not. The metrics of [22] does not consider an uncomputed output as a garbage output. According

Fig. 8 Reversible carry look-ahead adder proposed in [18]. a_i and b_i are the input numbers, c_0 is the carry input, S_i are the qubits of the result, C_{out} is the carry output and g_i the garbage outputs.

to the metrics proposed in [22], the proposal of [36] overcomes the adder of [29]. They present another circuit which reduces the delay (Fig. 7), but it has the same problems as the previous version.

One more reversible carry look-ahead adder is presented in [18]. It proposes a new technique for generating carry output (see Fig. 8). This circuit uses a new gate called Reversible Partial Adder (RPA) which has a quantum cost of 5 (and delay $5\triangle$) (Figs. 3(a) and 3(b) of [18]), and also has several Fredkin gates, which a cost of 5 each one (and delay $5\triangle$) for the 3 inputs case (Figs. 2(a) and 2(b) of [18]). Fig. 8 shows that the quantum cost of the circuit, for the case $N = 4$, includes 4 CNOT gates (4×1), 4 RPA gates (4×5) and 4 Fredkin gates ($4 \times X$), where X is the quantum cost of the 4-input Fredkin gates (their quantum cost is not covered by [18]). Considering a quantum cost of 5 for the 4-input Fredkin gate (this is the quantum cost they describe for the 3-input Fredkin gate), the circuit has a quantum cost of $4\times1 + 4\times5 + 4\times5 = 44$. Adding the extra cost of $2\times N$ to act as a converter, it has a quantum cost of 52. Moreover, the garbage outputs have not been uncomputed like in [29].

5.2 Comparison between the proposed circuit and the most efficient circuits

In this subsection, the results of a comparative analysis between the most efficient circuits to convert signed binary numbers to two's complement of N digits and our proposal are discussed.

Table 2 shows the comparison in terms of quantum costs for the conversion of numbers of N digits for [6], [36] and the proposed circuit. This table takes

into account the necessary operations so that the adders of [6] and [36] can make the conversion into two's complement.

The circuit of [6] (year 2004) is less competitive than [36] (year 2013). However, it is still better than the circuits studied in the previous subsection in terms of delay and quantum cost. It has a quantum cost of $28N - 15w(N) - 15log(N) - 6$. The circuit proposed in [36] cannot have input carry, and it has several ancilla inputs to improve the delay and quantum cost. It has no garbage outputs. The complete circuit has $4N - 3w(N) - 3logN$ Toffoli gates (the Toffoli gate has a quantum cost of 5 [26], or 3 two-qubits gates according to [15]), $N-1$ Peres gates (the Peres gate has a quantum cost of 4 [36]) and $2N$ CNOT gates, that is, it has a quantum cost of $26N - 15w(N) - 15log(N - 4)$. It contains less gates than the circuits presented in [6]. On the other hand, our proposed circuit improves the quantum cost of [36] thanks to the changes explained in Section 4. Results in Table 2 shows that the proposed converter improves in terms of quantum costs with respect to the use of general adders to compute the two's complement.

N	[6]	[36]	Proposed circuit	Improvement(%)
4	69	63	41	35
6	105	95	55	42
8	175	160	101	37
10	214	196	119	40
16	399	369	236	36
32	864	802	521	35
64	1869	1743	1166	33
128	3714	3460	2291	34
256	7539	7029	4676	33
512	15204	14182	9461	33

Table 2 Comparison of quantum costs for the conversion of numbers of N digits. Works [6] and [36] include extra cost of $2 \times N$ (N to transform a into $\bar{a}$ and N to restore a and avoid garbage outputs) to act as a converter. The improvement column shows the percentage of improvement of our proposal with respect to [36].

Table 3 shows a comparison of the delay, number of inputs and garbage outputs of some of the most relevant adder circuits in the literature. [36] has a delay of $logN + logN/3 + 2\triangle$, whereas the circuit of [6] has a delay of $logN + logN/3 + 7\triangle$. However, to perform $\bar{a} + 1$, the inversion of a with Pauli-X gates and another inversion to evade garbage outputs are necessary. This requires two extra levels of depth, so the final delays are $logN + logN/3 + 4\triangle$ and $logN + logN/3 + 9\triangle$, respectively for [36] and [6]. In Table 3, the logic depth of the circuits includes the necessary changes to allow them to make the conversion into two's complement. These changes involve to negate a at the beginning and to restore it at the end, to avoid garbage outputs. Furthermore, Table 3 shows that the proposed converter optimizes the number of inputs of the circuit and the answer delay. Therefore, our proposal improves converters based not only on quantum gates, such as [3] ($O(N)$), but also on quantum adders, such as [6,36], in terms of answer delay.

Circuit	Delay $\triangle$	Normal inputs	Ancilla inputs	Garbage outputs
[6]	$logN + logN/3 + 9$	$2N$	$5N/4$	0
[36]	$logN + logN/3 + 4$	$2N$	$5N/4$	0
Proposed circuit	$logN + logN/3 + 1$	N	$5N/4 - 9$	0

Table 3 Comparison of logic depth for N-digit numbers. Works [6] and [36] include two extra levels (one to transform a into $\bar{a}$ and other to restore a and avoid garbage outputs) to act as a converter.

6 Conclusions

In this paper, a reversible circuit which is capable of computing the conversion from signed numbers to two's complement has been presented. This converter is an adaptation of a reversible out-of-place carry look-ahead adder presented in [36], simplifying it to the specific operation $\bar{a} + 1$ (being a the number to be converted). We have carried out a deep analysis of the existing converter and adder circuits (current circuits that allow conversion from signed numbers to two's complement) to find the best ones considering a solid metric. We have justified that [6,36] are the best adders in terms of delay and quantum cost comparing them with the most modern circuits.

Once the best circuits have been identified, we have used them to design our proposal and, later, to compare the obtained results by all the studied circuits. Obtained results have shown that our proposed circuit outperforms the existing ones in terms of delay. The circuit improves the delay of [36] since all the Peres gates have been removed and several Toffoli gates have been replaced or simplified. Moreover, the number of normal input qubits has been reduced by half since the operations associated with the deleted inputs have been simplified.

An additional advantage of our proposal is that it does not contain any garbage output, therefore the circuit could be entangled with any other reversible circuit which needs to operate with two's complement. As future work, we are planning to implement a new carry look-ahead converter to compute the two's complement of a number.

References

1. Baugh, C.R., Wooley, B.A.: A two's complement parallel array multiplication algorithm. IEEE Transactions on Computers **100**(12), 1045–1047 (1973)
2. Chaudhuri, A., Sultana, M., Sengupta, D., Chaudhuri, A.: A novel reversible two's complement gate (tcg) and its quantum mapping. In: Devices for Integrated Circuit (DevIC), 2017, pp. 252–256. IEEE (2017)

3. Chaudhuri, A., Sultana, M., Sengupta, D., Chaudhuri, C., Chaudhuri, A.: A reversible approach to twos complement addition using a novel reversible tcg gate and its 4 dot 2 electron qca architecture. Microsystem Technologies pp. 1–11 (2018)
4. Cho, H., Swartzlander Jr, E.E.: Adder and multiplier design in quantum-dot cellular automata. IEEE Transactions on Computers **58**(6), 721–727 (2009)
5. Cuccaro, S.A., Draper, T.G., Kutin, S.A., Moulton, D.P.: A new quantum ripple-carry addition circuit. arXiv preprint quant-ph/0410184 (2004)
6. Draper, T.G., Kutin, S.A., Rains, E.M., Svore, K.M.: A logarithmic-depth quantum carry look-ahead adder. arXiv preprint quant-ph/0406142 (2004)
7. Gupta, A., Singla, P., Gupta, J., Maheshwari, N.: An improved structure of reversible adder and subtractor. arXiv preprint arXiv:1306.1889 (2013)
8. Haghparast, M., Jassbi, S.J., Navi, K., Hashemipour, O.: Design of a novel reversible multiplier circuit using hng gate in nanotechnology. In: World Appl. Sci. J. Citeseer (2008)
9. Hung, W.N., Song, X., Yang, G., Yang, J., Perkowski, M.: Optimal synthesis of multiple output boolean functions using a set of quantum gates by symbolic reachability analysis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems **25**(9), 1652–1663 (2006)
10. Islam, M.S., Rahman, M.M., Begum, Z., Hafiz, M.Z.: Fault tolerant reversible logic synthesis: Carry look-ahead and carry-skip adders. In: Advances in Computational Tools for Engineering Applications, 2009. ACTEA'09. International Conference on, pp. 396–401. IEEE (2009)
11. Khosropour, A., Aghababa, H., Forouzandeh, B.: Quantum division circuit based on restoring division algorithm. In: 2011 Eighth International Conference on Information Technology: New Generations, pp. 1037–1040. IEEE (2011)
12. Kianpour, M., Sabbaghi-Nadooshan, R.: Novel 8-bit reversible full adder/subtractor using a qca reversible gate. Journal of Computational Electronics **16**(2), 459–472 (2017)
13. Koren, I.: Computer arithmetic algorithms. AK Peters/CRC Press (2001)
14. Lanyon, B.P., Barbieri, M., Almeida, M.P., Jennewein, T., Ralph, T.C., Resch, K.J., Pryde, G.J., O'Brien, J.L., Gilchrist, A., White, A.G.: Simplifying quantum logic using higher-dimensional Hilbert spaces. Nature Physics **5**(2), 134–140 (2009).
15. Lemr, K., Bartkiewicz, K., Cernoch, A., Duek, M., Soubusta, J.: Experimental implementation of optimal linear-optical controlled-unitary gates. Physical review letters **114**(15), 153602 (2015).
16. Li, R., Alvarez-Rodriguez, U., Lamata, L., Solano, E.: Approximate quantum adders with genetic algorithms: an ibm quantum experience. Quantum Measurements and Quantum Metrology **4**(1), 1–7 (2017)
17. Ling, H.: High-speed binary adder. IBM Journal of Research and Development **25**(3), 156–166 (1981)
18. Lisa, N.J., Babu, H.M.H.: Design of a compact reversible carry look-ahead adder using dynamic programming. In: VLSI Design (VLSID), 2015 28th International Conference on, pp. 238–243. IEEE (2015)
19. Markov, I.L., Saeedi, M.: Constant-optimized quantum circuits for modular multiplication and exponentiation. arXiv preprint arXiv:1202.6614 (2012)
20. Mazumder, M.: Synthesis of quantum circuit for full adder using khan gate. Quantum **6**(6) (2017)
21. Moghimi, S., Reshadinezhad, M.R.: A novel 4× 4 universal reversible gate as a cost efficient full adder/subtractor in terms of reversible and quantum metrics. International Journal of Modern Education & Computer Science **7**(11) (2015)
22. Mohammadi, M., Eshghi, M.: On figures of merit in reversible and quantum logic designs. Quantum Information Processing **8**(4), 297–318 (2009)
23. Mokhtari, D., Rezai, A., Rashidi, H., Rabiei, F., Emadi, S., Karimi, A.: Design of novel efficient full adder architecture for quantum-dot cellular automata technology. Facta Universitatis, Series: Electronics and Energetics **31**(2), 279–285 (2018)
24. Montaser, R., Younes, A., Abdel-Aty, M.: New design of reversible full adder/subtractor using r gate. arXiv preprint arXiv:1708.00306 (2017)
25. Murali, K., Sinha, N., Mahesh, T., Levitt, M.H., Ramanathan, K., Kumar, A.: Quantum-information processing by nuclear magnetic resonance: Experimental implementation of half-adder and subtractor operations using an oriented spin-7/2 system. Physical Review A **66**(2), 022313 (2002)

26. Nielsen, M.A., Chuang, I.L.: Quantum computation and quantum information 10th edition (2017)
27. Orts, F., Ortega, G., Garzón, E.M.: A quantum circuit for solving divisions using grovers search algorithm. In: Proc. 18th Int. Conf. Comput. Math. Method. Sci. Eng (2018)
28. Orts, F., Ortega, G., Garzón, E.M.: A faster half subtractor circuit using reversible quantum gates. Baltic Journal of Modern Computing **7**(1), 99–111 (2019)
29. Rahmati, M., Houshmand, M., Kaffashian, M.H.: Novel designs of a carry/borrow look-ahead adder/subtractor using reversible gates. Journal of Computational Electronics **16**(3), 856–866 (2017)
30. Shukla, V., Singh, O., Mishra, G., Tiwari, R.: Design of a 4-bit 2s complement reversible circuit for arithmetic logic unit applications. In: The International Conference on Communication, Computing and Information Technology (ICCCMIT), Special Issue of International Journal of Computer Applications, pp. 1–5 (2012)
31. Takahashi, Y., Kunihiro, N.: A linear-size quantum circuit for addition with no ancillary qubits. Quantum Information & Computation **5**(6), 440–448 (2005)
32. Takahashi, Y., Kunihiro, N.: A fast quantum circuit for addition with few qubits. Quantum Information & Computation **8**(6), 636–649 (2008)
33. Takahashi, Y., Tani, S., Kunihiro, N.: Quantum addition circuits and unbounded fan-out. Quantum Information & Computation **10**(9), 872–890 (2010)
34. Talib, G.H.B., El-Maleh, A.H., Sait, S.M.: Design of fault tolerant adders: A review. Arabian Journal for Science and Engineering **43**(12), 6667–6692 (2018)
35. Thapliyal, H.: Mapping of subtractor and adder-subtractor circuits on reversible quantum gates. In: Transactions on Computational Science XXVII, pp. 10–34. Springer (2016)
36. Thapliyal, H., Jayashree, H., Nagamani, A., Arabnia, H.R.: Progress in reversible processor design: a novel methodology for reversible carry look-ahead adder. In: Transactions on Computational Science XVII, pp. 73–97. Springer (2013)
37. Theresal, T., Sathish, K., Aswinkumar, R.: A new design of optical reversible adder and subtractor using mzi. Published at International Journal of Scientific and Research Publications (IJSRP) **5**(4) (2015)
38. Toffoli, T.: Reversible computing. In: International Colloquium on Automata, Languages, and Programming, pp. 632–644. Springer (1980)
39. Wang, F., Luo, M., Li, H., Qu, Z., Wang, X.: Improved quantum ripple-carry addition circuit. Science China Information Sciences **59**(4) (2016)
40. Wang, J., Choi, K.: A carry look-ahead adder designed by reversible logic. In: SoC Design Conference (ISOCC), 2014 International, pp. 216–217. IEEE (2014)
41. Williams, C.P.: Explorations in quantum computing. Springer Science & Business Media (2010)