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Optimal fault-tolerant quantum comparators for image binarization.

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Abstract Quantum image processing focuses on the use of quantum computing in the field of digital image processing. In the last few years, this technique has emerged since the properties inherent to quantum mechanics would provide the computing power required to solve hard problems much faster than classical computers. Binarization is often recognized to be one of the most important steps in image processing systems. Image binarization consists of converting the digital image into a black and white image, so that the essential properties of the image are preserved. In this paper, we propose a quantum circuit for image binarization based on two novel comparators. These comparators are focused on optimizing the number of T gates needed to build them. The use of T gates is essential for quantum circuits to counteract the effects of internal and external noise. However, these gates are highly expensive, and its slowness also represents a common bottleneck in this type of circuit. The proposed quantum comparators have been compared with other state-of-the-arts comparators. The analysis of the implementations have shown our comparators are the best option when noise is a problem and its reduction is mandatory.

Keywords Quantum computing · Quantum image binarization · Quantum comparator

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1 Introduction

Quantum computing has emerged as a new and promising science that has new challenges. One of them is that quantum computing is counterintuitive since it has some interesting but not intuitive features like entanglement and quantum parallelism [13]. Just a few years ago, the interest of researchers in quantum computing was focused on mathematical and physical fields because of the lack of real quantum computers and efficient quantum simulators. Recently, IBM, D-Wave, Google, and other important organizations have built real and functional quantum computers [18]. Moreover, Microsoft, QuTech, Intel, Amazon and other vendors have opened new services based on several kind of computers and architectures [5].

There are different paradigms in quantum computing. For instance, quantum annealers, like the D-Wave machine, are focused on solving problems that can be expressed as energy minimization [18]. On the other hand, topological quantum computers work with two-dimensional quasiparticles to process quantum information, which allows a better resilience against perturbations [17] (nevertheless, topological quantum computers have not even been built nowadays, and only theoretical models have been developed. Furthermore, several ambitious quantum simulators have been developed recently, for example, QuEST, ProjectQ and myQLM [6,8,19].

Despite the fact that quantum technology is very innovative and powerful, there are many challenges to make quantum computing be practical. One of its main limitations is that quantum computers are difficult to program because their computational models are quite different from the classical one. The most well-known model is based on quantum circuits, where each specific procedure involves the design of particular quantum circuits. Because of the scarcity of quantum resources and the strong sensibility of the quantum computers to noise, the design of quantum circuits should be optimized in terms of number of resources and fault-tolerance. Therefore, an active research line is the optimal design of basic quantum operations involved in complex algorithms [14,15,16, 20].

Quantum image processing (QIMP) is an interdisciplinary subject between quantum computation and image processing. In recent years, along with the bright future of quantum computers, QIMP has become a hot research field. Combining quantum mechanics with image processing is an effective approach to improve the processing speed of images [21]. Its main functionality is to capture, manipulate and recover quantum images by means of the quantum computing [27]. According to the literature, QIMP techniques could improve classical processing algorithms in terms of performance, guaranteed security and minimal storage requirements [7,27]. The benefits of such techniques have been demonstrated in a wide number of applications such as image classification, morphology, registration, synthesis, segmentation, filtering, and pseudocolor [28].

In this work the focus is the quantum image binarization. The binarization is a crucial step in many image processing techniques. Binarization is a simple thresholding process over the image where the pixels with gray-levels lower than a given threshold are classified into a class (i.e. the background), and all the remaining pixels into another (i.e, the foreground). It is well known that the key of a binarization process is the comparison between each pixel and the threshold value. So, our intention is to design an efficient circuit to compare two quantum logic states and to identify whether they are equal or, otherwise, which of them is the largest [22].

There are already many classical methods proposed for image binarization [11]. However, quantum image processing provides an opportunity for faster image processing; therefore, recently received some attention in the quantum research community. Probably, the first proposed quantum comparator for image binarization is presented in [1]. A novel 8-bit half comparator was proposed in the context of binarization in [25], and in [26] it was optimized by rearranging the quantum gates. A quantum version of the Otsu's threshold selection method which contains image binarization procedure was designed in [10]. These publications showed that quantum computing offers a potential solution to efficiently deal with image binarization; however, currently, research content is very limited.

In this work, we propose two fault-tolerant comparators focused on optimizing the number of T gates. Quantum circuits are very sensitive to external and internal noise, therefore the noise reduction and fault tolerance are two of the most important objectives in quantum computing. The T gates are used to make possible the use of error-correcting codes to ensure fault-tolerance in quantum circuits. However, they are more expensive than other gates in terms of space and time cost due to, precisely, their increased tolerance to noise errors [12, 29]. In the design of quantum circuits, it is very relevant to specify the metrics used to evaluate the efficiency of such circuits. In order to evaluate our proposed and state-of-the-arts quantum circuits, we have considered the number of T gates a circuit has (T-count), the number of steps involving T gates, that is, the number of T gates which must be computed sequentially (T-depth) and the number of ancilla qubits.

The main contributions of the paper can be summarized as follows: (1) Development of a fault-tolerant quantum comparator; (2) Integration of the comparators in a circuit for image binarization that can be used as part of QIMP circuits that outperforms their classical counterparts [3, 2, 23]; and, (3) Evaluation of the proposed and other state-of-the-arts quantum comparators.

The manuscript is written as it follows. Section 2 describes the quantum image binarization circuit design. In Section 3 we propose efficient quantum comparators. In Section 4, a comparative evaluation is carried out between our comparator and others of the state-of-the-art. Finally, we present the conclusions in Section 5.

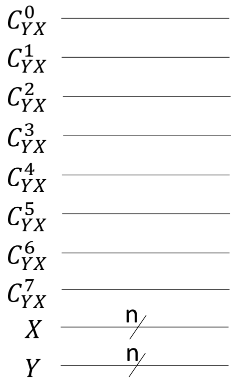

Fig. 1: A 2^3-color range image represented in NEQR. $C^7_{YX}...C^0_{YX}$ is the codification of the pixel, and XY the location.

2 Quantum image binarization circuit design

Our proposal is based on the binarization algorithm described by Xia et al [25]. This algorithm assumes that the image to be binarized is encoded in NEQR representation (Novel Enhanced Quantum Representation) [30]. In the NEQR representation, an image is represented according to the following equation:

$$|C_{YX}\rangle = \frac{1}{2^n}\sum_{Y=0}^{2^n-1}\sum_{X=0}^{2^n-1}|C^{q-1}_{YX}C^{q-2}_{YX}...C^1_{YX}C^0_{YX}\rangle \otimes |YX\rangle \tag{1}$$

Where $|C^{q-1}_{YX}C^{q-2}_{YX}...C^1_{YX}C^0_{YX}\rangle$ codifies the value of the pixel (Y,X), n is related to the size of the image (it is a $2^n \times 2^n$ image), and q defines the color range as 2^q. YX encodes the spatial location of the pixel. A visual example of this representation for the 2^3 color range case is shown in Fig. 1.

For the sake of clarity, Algorithm 1 shows the pseudo-code for the 2^3 color range case. This algorithm needs two external values for each pixel of the image to be binarized: the codification $I = C^{q-1}_{YX}C^{q-2}_{YX}...C^1_{YX}C^0_{YX}$ of the pixel, and a threshold value which is used to decide whether the pixel should be black or white. The algorithm consists of two steps:

- The first part compares C_{YX} with the threshold value b. There is no need to perform a complete comparison since it is only needed to compute if $C_{YX} < b$ or $C_{YX} \geq b$. Therefore, a half comparator can be used. It should return $c = 1$ if $C_{YX} < b$, and 0 otherwise.
- The second part changes $C^{q-1}_{YX}C^{q-2}_{YX}...C^1_{YX}C^0_{YX}$ to 0 if $c = 1$, or to 1 if $c = 0$. That is, the algorithm sets the pixel as black if its original value is lesser than the threshold value, or sets it as white if its original value is greater or equal than the threshold value.

A quantum circuit to implement Algorithm 1 is shown in Fig. 2. On the one hand, the implementation of the second part of this circuit involves several

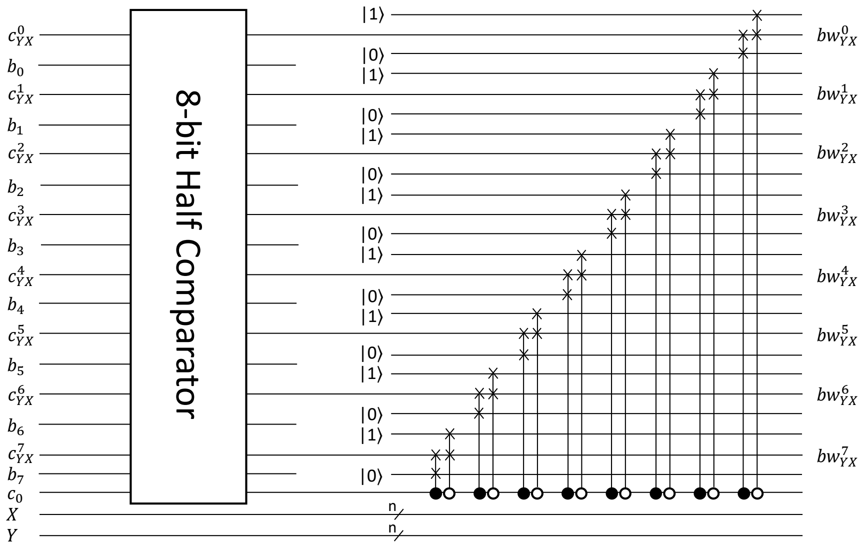

Fig. 2: Circuit implementation for Algorithm 1. This algorithm consists of two parts: a comparison between the pixel C_{YX} and the threshold b; and the assignment of the value 0 or 1 using swap gates to the pixel, according to the result of the previous comparison.

swap gates. Such gates set the qubits of the pixel to 0 or 1 depending on the result of the comparison. The operation may seem simple, but it involves n inputs in state $|0\rangle$ and n in state $|1\rangle$. These states are swapped with the original pixel value under the conditions described in the previous paragraph. Also, and since we do not know beforehand into which group of inputs ($|0\rangle$ or $|1\rangle$) the original values of the pixels will be exchanged, we can therefore consider that we have $2n$ garbage outputs. On the other hand, the implementation of the half comparator is far from trivial [9, 24, 25]. This implementation is discussed in the next section.

Algorithm 1: Image binarization in quantum computing proposed in [25].

Result: A binary image bw.
$b = |b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0\rangle$;
$I = |C^7_{YX} C^6_{YX} C^5_{YX} C^4_{YX} C^3_{YX} C^2_{YX} C^1_{YX} C^0_{YX}\rangle$;
$c_0 = |0\rangle$;
if $I < b$ **then**
  $c_0 = |1\rangle$;
end
Swap each quantum logic bit in I with c_o;
$bw = I$;
return bw;

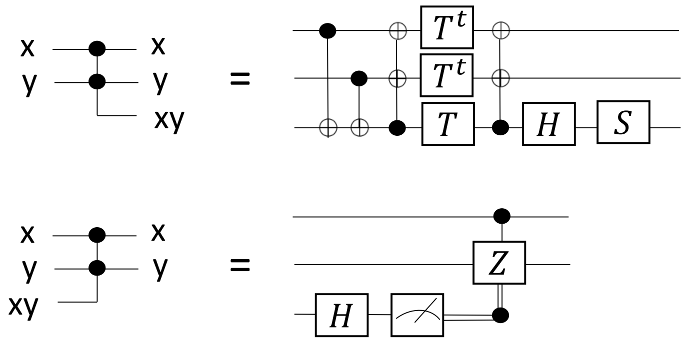

Fig. 3: Temporary logical-AND gate and its uncomputation.

3 Proposed quantum comparators

In this section we describe our proposed comparators. Two comparators have been developed as part of this work. The first one is focused on reducing the T-count, and the second comparator is focused on reducing the T-depth. They use the temporary logical-AND gate [4] in order to reduce the number of involved T gates. This gate performs an AND operation of two inputs (qubits), saving the result in an ancilla qubit. This is similar to the Toffoli gate, but the T-count of the temporary logical-AND is 4, and its T-depth is 2 (for the Toffoli gate, these values are 7 and 3, respectively). Moreover, the uncomputation of the temporary logical-AND does not involve T gates, whereas the uncomputation of the Toffoli gate involves another Toffoli gate. The temporary logical-AND gate (and its uncomputation gate) is shown in Fig. 3.

As it will be shown later, both of them have lower T-count and T-depth than existing quantum comparators.

The first proposed comparator is shown in Fig. 4. It is based on the methodology of the adder developed by Gidney in 2018 [4], which is the best adder in terms of T-count currently available [14]. The comparison between two bit strings a and b is carried out performing the operation $a - b$. This operation can be performed using an adder, computing $\overline{\overline{a} + b}$. Actually, we are only interested in the sign of the operation, so that we can determine that a is lower than b if the sign of $a - b$ is negative, or that a is greater (or equal) than b if the result is positive. Therefore, several simplifications can be done to perform only the computation of the sign. The circuit can be reproduced for any size n of bits following these steps:

- For $i = 0$ to $i = n - 1$, to apply a Pauli-X gate at every bit a_i to perform $\overline{a}$. These operations are computed in parallel as it is shown in circuit example of Fig. 4.
- Perform the operation $a_0 b_0$ using a temporary logical-AND gate instead of a Toffoli gate to save T-count and T-depth. Each temporary logical-AND will require an extra qubit, which must be initialized to the state $\frac{1}{\sqrt{2}}(|0\rangle + e^{\frac{i\pi}{4}} |1\rangle)$. These ancilla qubits are marked as A in Fig. 4.

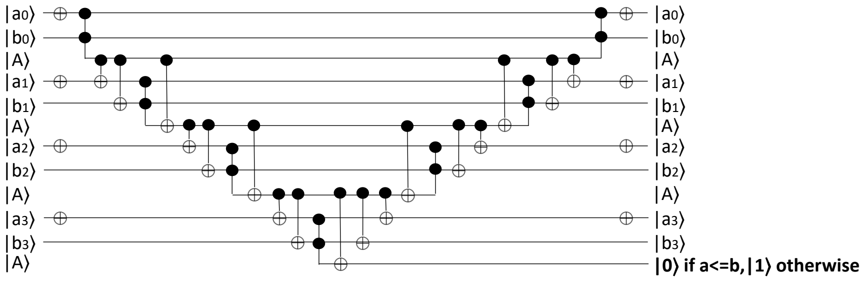

Fig. 4: Example of the first proposed comparator for the $n = 4$ case. This circuit is focused on reducing the T-count. a_i and b_i are the bit strings to be compared. A are ancilla qubits.

- For $i = 1$ to $i = n-1$, apply two CNOT gates to compute $(a_{i-1}b_{i-1}) \oplus a_i$ and $(a_{i-1}b_{i-1}) \oplus b_i$. Then, to apply a temporary logical-AND to compute a_ib_i. Finally, to apply another CNOT gate to perform $(a_{i-1}b_{i-1}) \oplus (a_ib_i)$. Each step of the loop must be computed sequentially.
- The result is given by the last operation of the last iteration computed in the previous step. However, uncomputation is required to avoid garbage outputs. Applying two CNOT gates to perform $(a_{n-2}b_{n-2}) \oplus a_{n-1}$ and $(a_{n-2}b_{n-2}) \oplus b_{n-1}$.
- For $i = n-2$ to $i = 1$, apply a CNOT gate to perform $(a_{i-1}b_{i-1}) \oplus (a_ib_i)$. Then, apply the uncomputation circuit for the logical and operation at a_ib_i. Finally, apply two CNOT gates at $(a_{i-1}b_{i-1}) \oplus a_i$ and $(a_{i-1}b_{i-1}) \oplus b_i$. Again, each step of the loop must be computed sequentially.
- Finally, for $i = 0$ to $i = n-1$ apply a Pauli-X gate at every bit a_i to uncompute them. All the qubits except the one that contains the result have been uncomputed.

The second proposed comparator is shown in Fig. 5. It is based on the methodology of the adder developed by Thapliyal et al. in 2020 [20], which is the best adder in terms of T-depth currently available [14]. Again, the comparison is performed computing $\overline{\overline{a} + b}$. This circuits involves the use of a huge amount of ancilla qubits to achieve a logarithmic T-depth since every and operation is performed using temporary logical AND gates. These gates could be replaced totally or partially to reduce the number of ancilla inputs. However, this will increase the T-depth and also the T-count of the circuit. The comparator can be reproduced for any size n of bits following these steps:

- For $i = 0$ to $i = n-1$, to apply a Pauli-X gate at every bit a_i to perform $\overline{a}$. Then, apply a temporary logical-AND gate to calculate a_ib_i. According to the original adder, this value will be renamed as $g[i, i+1]$.
- For $i = 1$ to $i = n-1$, to apply a CNOT gate at $a_i \oplus b_i$. This value will be renamed as $p[i, i+1]$.

- For $i = 2$ to $i = log(n) - 1$, and for $j = 1$ to $j = \frac{n}{2^i} - 1$, apply a temporary logical AND at locations $p[x, y], p[y, z]$, being $x = 2^i j$, $y = 2^i j + 2^i$, and $z = 2^i j + 2^{i-1}$, respectively.
- For $i = 1$ to $i = log(n)$, and for $j = 0$ to $j = \frac{n}{2^i} - 1$, apply a temporary logical AND and an uncomputation gate at locations $g[x, y], g[y, z]$, being $x = 2^i j$, $y = 2^i j + 2^i$, and $z = 2^i j + 2^{i-1}$, respectively.
- For $i = log(\frac{2n}{3})$ to $i = 1$, and for $j = 1$ to $j = \frac{n-2^{i-1}}{2^i}$, to apply a temporary logical-AND and its uncomputation at g[0,x], p[x,y] y g[x,y], being $x = 2^i j$, and $y = 2^i j + 2^{i-1}$, respectively.
- For $i = 1$ to $n - 1$, to apply a CNOT gate at p[i, i+1] and g[0, i].
- For $i = 1$ to $n - 1$, to apply a CNOT gate at p[0, 1] and the corresponding ancilla input. Steps 3, 2, and 1 (in this order) must be computed again to uncompute garbage outputs.

4 Analysis and comparison

The proposed comparators consist of only four kind of gates: Pauli-X gates, CNOT gates, temporary logical-AND gates, and the uncomputation gate for the temporary logical-AND gate. Among these gates, only the temporary logical-AND involves T gates. Therefore, the T-count and the T-depth of our circuits can be obtained from the total number of temporary logical-AND gates they have and the number of temporary logical-AND gates that the circuits must compute sequentially, respectively. The T-count and the T-depth of the temporary logical-AND gate are 4 and 2, respectively (Fig. 3).

The first circuit involves n consecutive temporary logical-AND gates. Then, it has a T-count of $4n$ and a T-depth of $2n$. Since the circuit only uses the ancilla qubits involved in the logical-AND operations, it can be concluded that the first comparator needs n ancilla qubits. On the other hand, the second comparator involves $3n - 2W(n) - log(n)$ temporary logical-AND gates, being $W(n)$ the number of ones in the binary expansion of n. Therefore, its T-count is $12n - 8W(n) - 4log(n)$. The T-depth is not trivial to compute since the depth of the circuit, depends on the value of n. However, we have shown that the circuit grows logarithmically. Then, its T-depth can be set as $log(n)$.

Circuit Comparator	T-count	T-depth	Ancilla qubit
Xia et al. (2018) [24]	$14n$	$6n$	2
Xia et al. (2019) [25]	$14n - 7$	$6n - 3$	2
Li et al. (2020) [9]	$14n - 7$	$6n - 3$	1
Proposed comparator	$4n$	$2n$	n
Proposed comparator	$12n - 8W(n) - 4Log(n)$	$Log(n)$	$4n - 2W(n) - 2log(n)$

Table 1: Evaluation of comparators in terms of T-count, T-depth and Ancilla qubits as functions of n. $W(n)$ is the number of ones in the binary expansion of n.

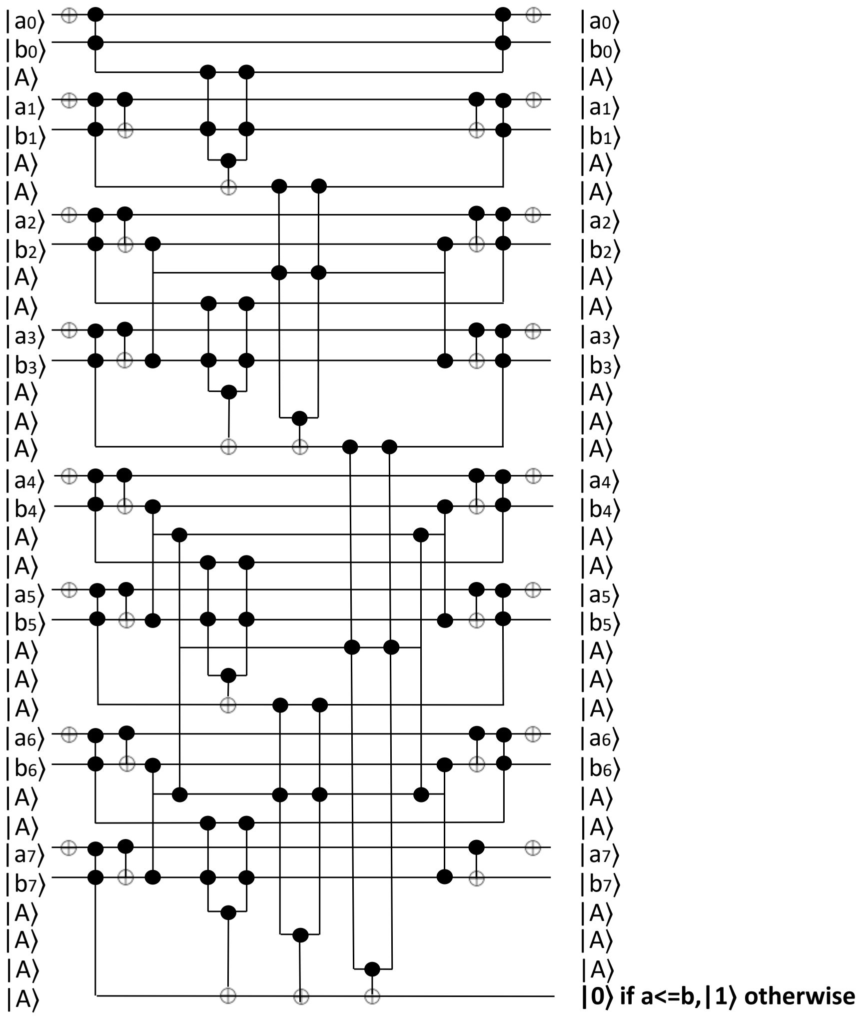

Fig. 5: Example of the second proposed comparator for the $n = 8$ case. This circuit is focused on reducing the T-depth. a_i and b_i are the bit strings to be compared. A are ancilla qubits.

Table 1 shows a comparison in terms of T-count, T-depth, and number of ancilla inputs between the most recent comparators in the state-of-the-art and our two proposed circuits. In terms of T-count and T-depth, it is shown that our circuits outperform the other comparators. Focusing on the T-count, the first proposed is the best option with a T-count of $4n$. The circuit with best T-count in the literature is the proposal of Li et al. [9]. This circuit has a T-count of $14n - 7$, which is a value three times greater than our proposal. Our second proposal has a T-count of $12n - 8W(n) - 4log(n)$, which is still better than the circuit of Li et al [9].

Focusing now in the T-depth, the only logarithmic circuit is our second proposal. The other comparators are lineal. Again, the circuit of Li et al. is the best option in the literature, with a T-depth of $6n - 3$. Our first proposal, with a T-depth of $2n$, also outperforms the circuit of Li et al.

However, the circuit of Li et al. [9] has an important feature: it is the best in terms of necessary qubits. It is the only comparator with a single ancilla qubit. In these terms, out best proposal is the first one with n ancilla qubits. Therefore, the circuit of Li et al. [9] improves us in $n - 1$ qubits.

5 Conclusion

In this paper, we continue the work started in [25] about binarization in quantum computing. In particular, we have improved a quantum circuit for binarization providing two novel comparators focused on the reduction of the internal and external noise. Although we work in a binarization framework, these comparators are valid for a general purpose.

Our two circuits are able to reduce the number of necessary T gates (with involves the reduction of the T-count and T-depth), thanks to the use of the temporary logical-AND gate proposed by [4], and also using the most efficient methodologies for noise reduction in quantum binary adders. Our first circuit is focused on the reduction of the T-count, and the second one is based on the reduction of the T-depth. However, the two circuits improve both in T-count and T-depth to the currently available circuits.

As a complement, we have carried out a comparison between our circuits and the most prominent comparators in the literature. The conclusions are that our circuits are the best option when noise is a problem and its reduction is mandatory. However, we also shown than the circuit proposed in Li et al. [9] is the best option when the focus is to minimize the number of qubits.

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